EGC220

Digital Logic Fundamentals

Programmable Logic Devices

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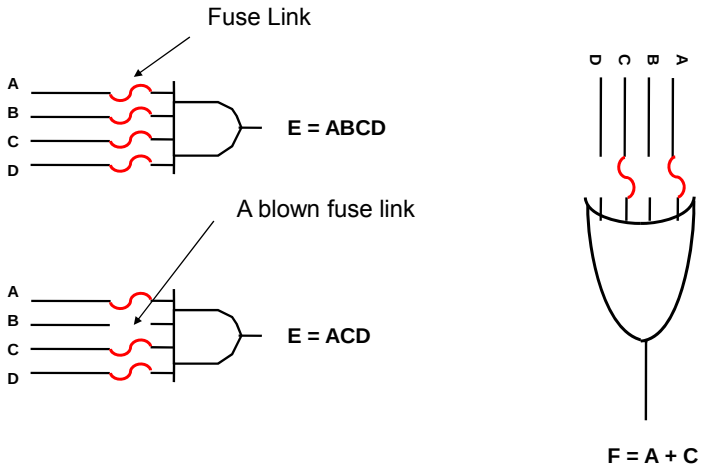
Introduction



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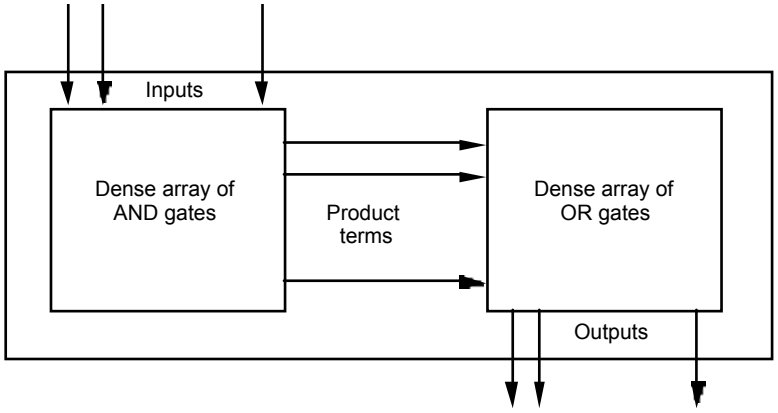
Basic PLDs

Programmable AND block followed by a programmable OR block

Programmable Array Block Diagram for Sum of Products Form



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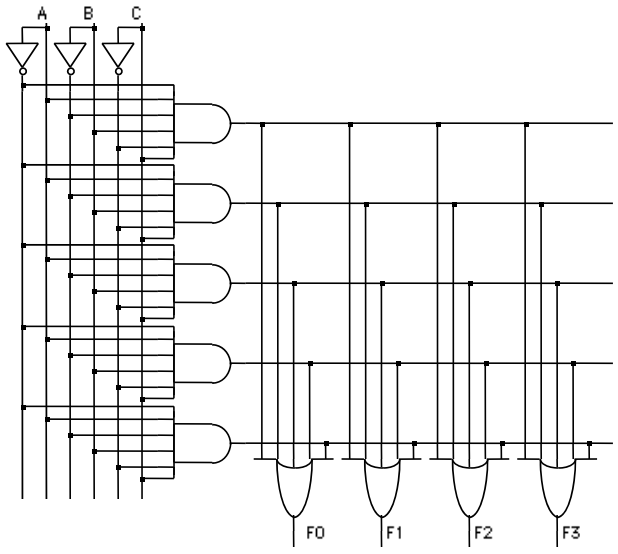
Basic PLDs

All possible connections are available before programming



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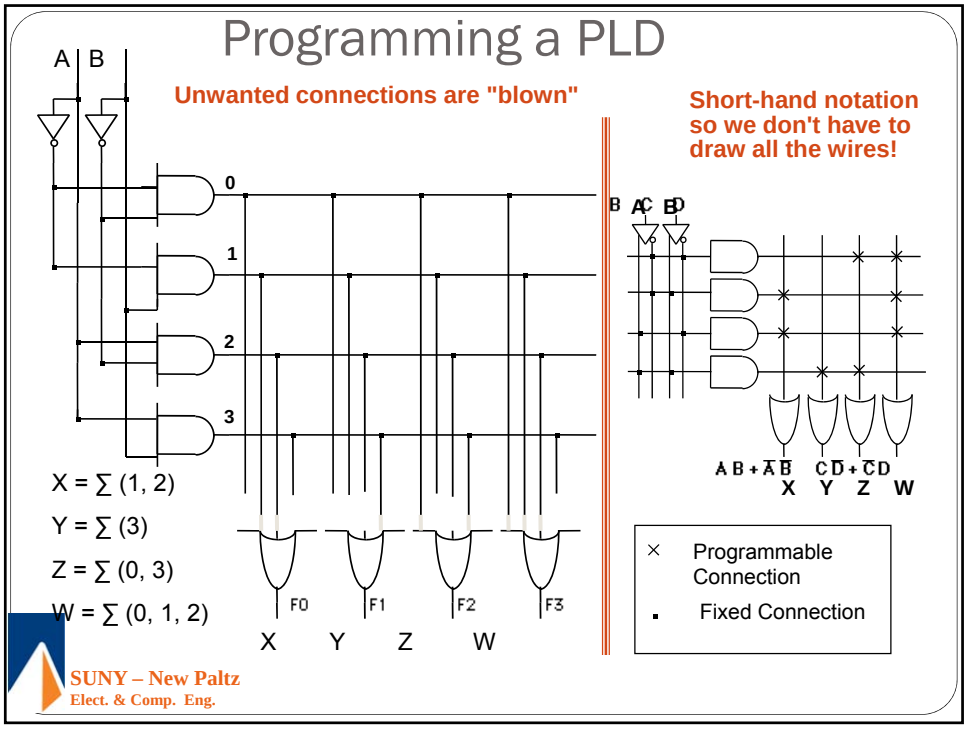
Programming a PLD
A B
Unwanted connections are "blown"
Short-hand notation so we don't have to draw all the wires!
0
1
2
3
X = ∑ (1, 2)
Y = ∑ (3)
Z = ∑ (0, 3)
W = ∑ (0, 1, 2)
F0
F1
F2
F3
X Y Z W
× Programmable Connection
▪ Fixed Connection
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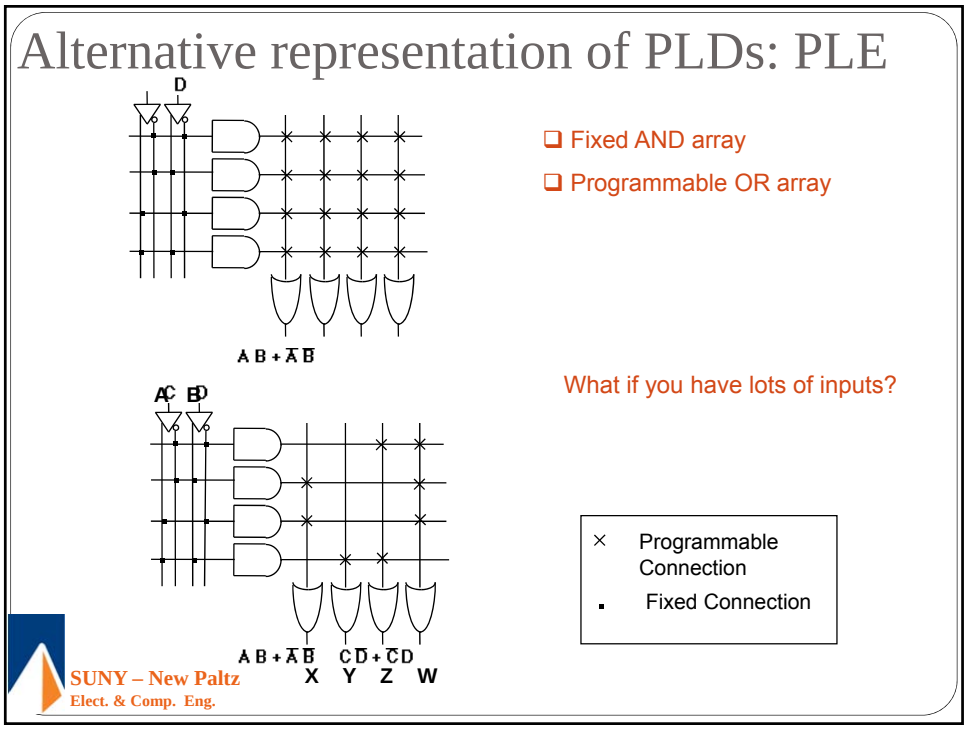
Alternative representation of PLDs: PLE
D
❑ Fixed AND array
❑ Programmable OR array
What if you have lots of inputs?
× Programmable Connection
▪ Fixed Connection
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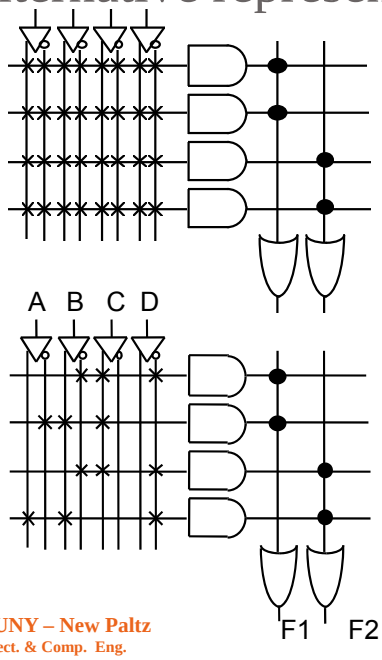
Alternative representation of PLDs: PAL



- Programmable AND array
- Fixed OR array

A given column of the OR array has access to only a subset of the possible product terms

× Programmable Connection
● Fixed Connection

F1 = B'CD' + A'BC

F2 = B'CD' + ABD'

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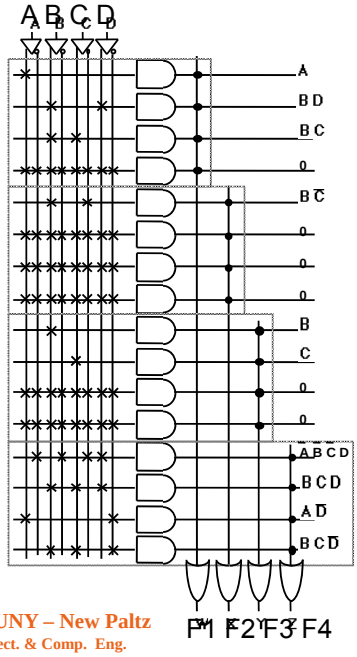
PALs with Four Product terms



Complete the following:

F1 =

F2 =

F3 =

F4 =

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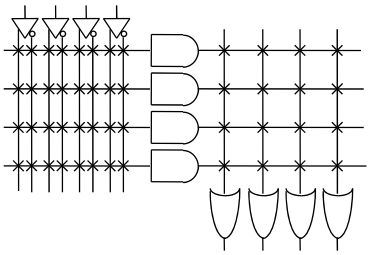
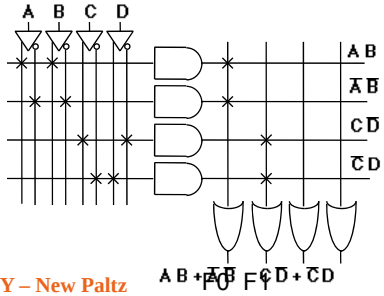
Alternative representation of PLDs: PLA



- Programmable AND array
- Programmable OR array

× Programmable Connection
● Fixed Connection



F0 = A B + A' B'
F1 = C D' + C' D

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Design Example using PLA

Multiple functions of A, B, C

F1 = A B C

F2 = A + B + C

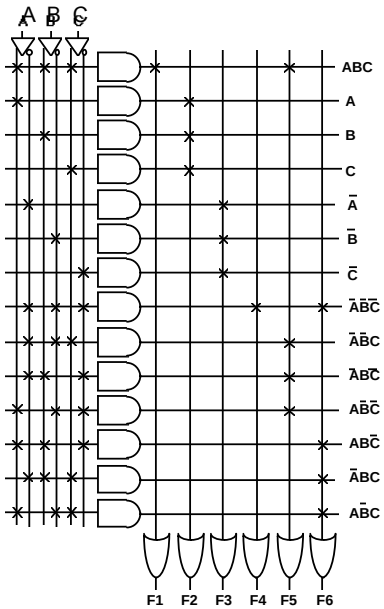
F3 = $\overline{A B C}$

F4 = $\overline{A + B + C}$

F5 = A ⊕ B ⊕ C

F6 = $\overline{A \oplus B \oplus C}$

What is difference between Programmable Array Logic (PAL) and Programmable Logic Array (PLA)?



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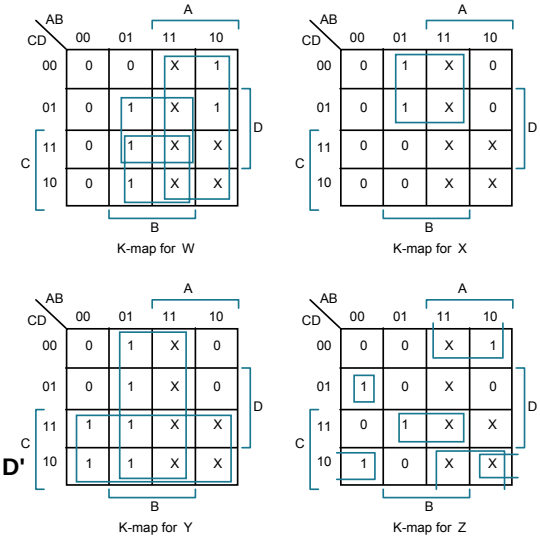
Design Example: BCD to Gray Code Converter

Truth Table

A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	1	1	1	0
0	1	1	0	1	0	1	0
0	1	1	1	1	0	1	1
1	0	0	0	1	0	0	1
1	0	0	1	1	0	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

K-maps



Minimized Functions:

W = A + B D + B C
X = B C'
Y = B + C
Z = A'B'C'D + B C D + A D' + B' C D'

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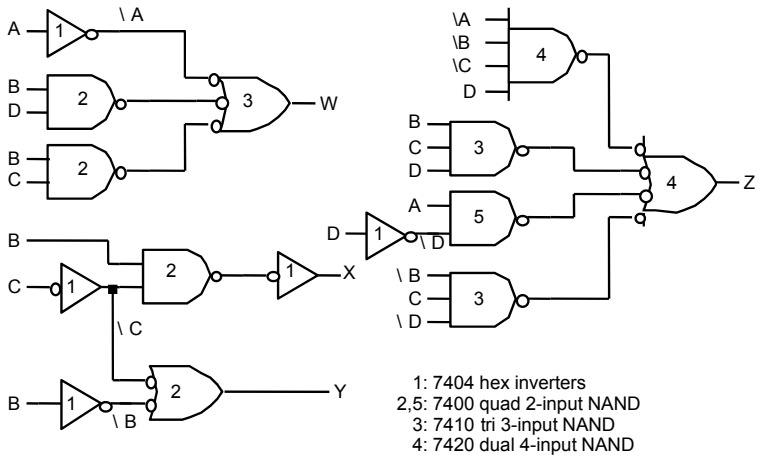
Code Converter Discrete Gate Implementation Using SSI



1: 7404 hex inverters
2,5: 7400 quad 2-input NAND
3: 7410 tri 3-input NAND
4: 7420 dual 4-input NAND

4 SSI Packages vs. 1 PLA/PAL Package!

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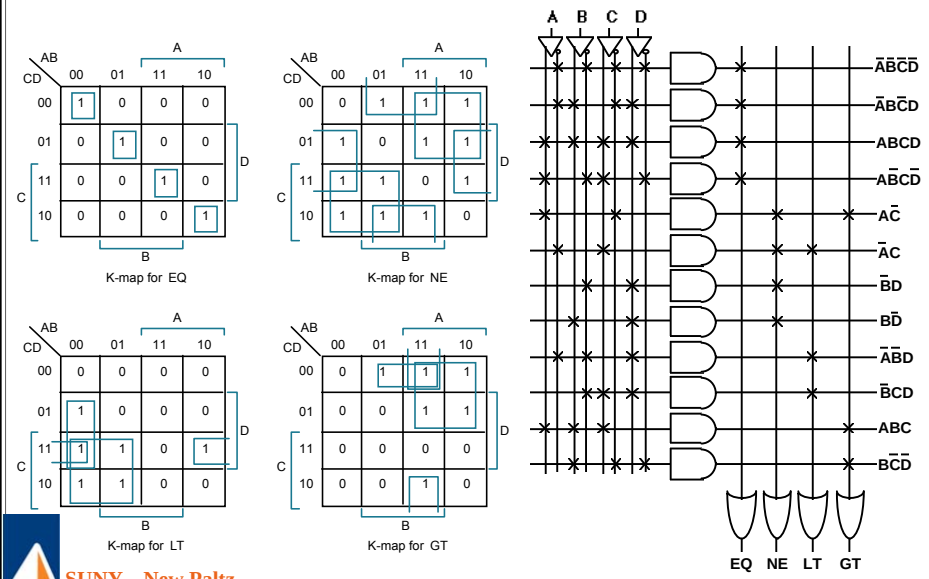
Another Example: Magnitude Comparator



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Key Advantage of PLA: Shared Product Terms

Example:

F0 = A + B' C'
F1 = A C' + A B
F2 = B' C' + A B
F3 = B' C + A

Personality Matrix

Product term	Inputs A B C	Outputs F_0 F_1 F_2 F_3
A B	1 1 -	0 1 1 0
$\bar{B}$ C	- 0 1	0 0 0 1
A $\bar{C}$	1 - 0	0 1 0 0
$\bar{B}\bar{C}$	- 0 0	1 0 1 0
A	1 - -	1 0 0 1

Reuse of terms

Input Side:
1 = asserted in term
0 = negated in term
- = does not participate

Output Side:
1 = term connected to output
0 = no connection to output

Finding shared product term not that easy for large design.

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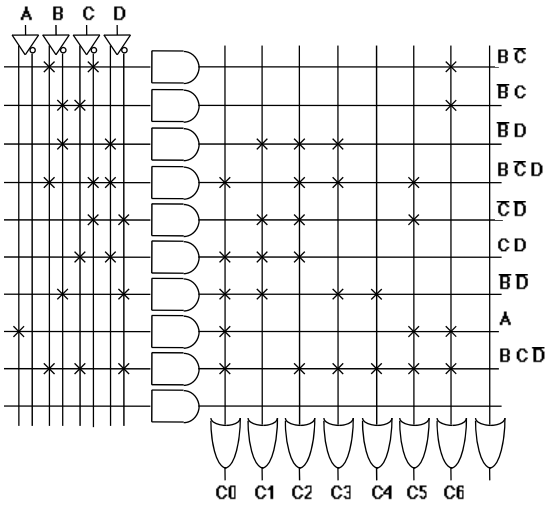
Combinational Logic BCD to 7 Segment Display Controller Problems

PLA Implementation



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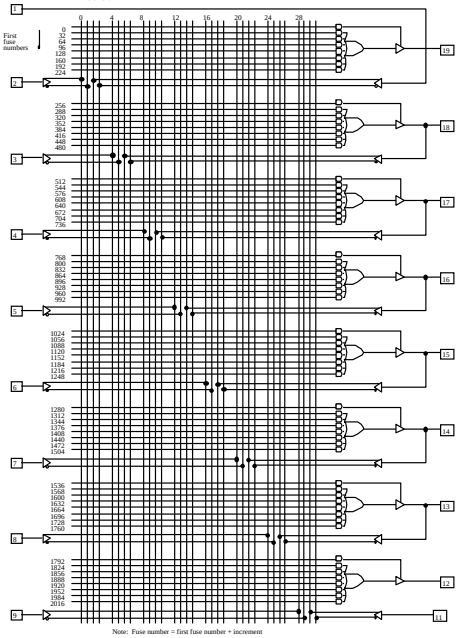
Actual PAL Device

16H8PAL:
- 16 inputs
- 8 outputs



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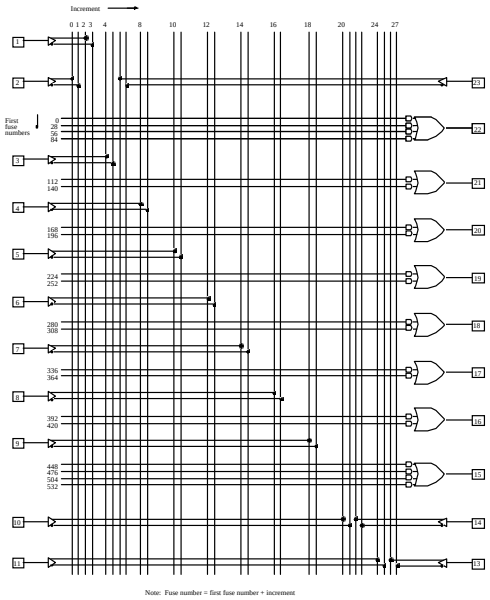
BCD to 7 Segment Display Controller on 16H8PAL



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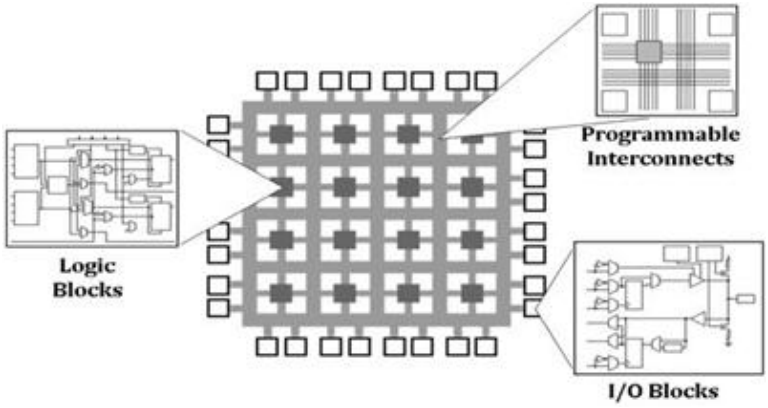
What about FPGA?

- Has millions of programmable gates organized into Logic Blocks
- Logic Blocks are interconnected using programmable



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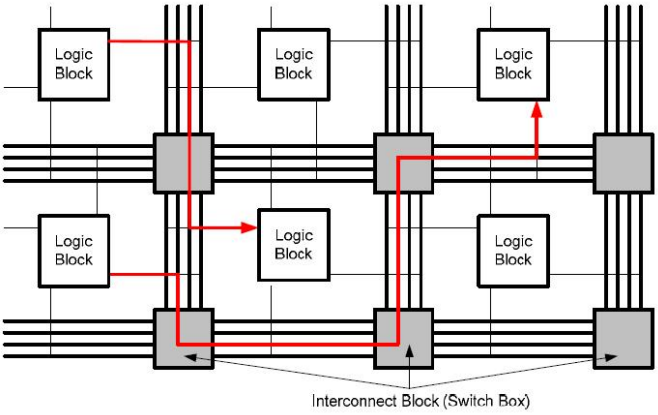
What about FPGA?

- Programmable interconnects using switch matrixes
- Several types of interconnects: short distance (local), long distances across chip,



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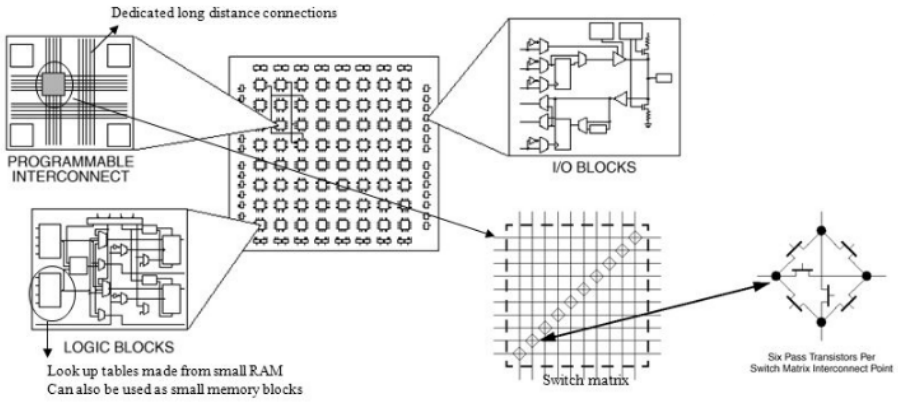
- FPGA's provide enormous design capabilities.



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